IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An apparatus comprising:

a common mode rejection amplifier including first and second input transistors to form a first differential input stage, and third and fourth input transistors to form a second differential input stage, the first and second differential input stages coupled in parallel;

a plurality of low pass filters coupled to the common mode rejection amplifier to produce a band pass amplifier response; and

an input ~~stage~~ amplifier having first and second differential outputs;

wherein the plurality of low pass filters comprises first and second low pass filters coupled to receive signals from the first differential output of the input amplifier, and third and fourth low pass filters coupled to receive signals from the second differential output of the input amplifier, and wherein the first and third low pass filters are coupled to provide signals to the first and second input transistors, respectively, of the first differential input stage, and the second and fourth low pass filters are coupled to provide signals to the third and fourth input transistors, respectively, of the second differential input stage. ~~the common mode rejection amplifier includes two parallel-coupled differential input stages coupled to the plurality of low pass filters.~~

2. (Canceled)

3. (Original) The apparatus of claim 1 wherein at least one of the plurality of low pass filters comprises a programmable low pass filter.

4-6. (Canceled)

7. (Previously Presented) The apparatus of claim 1 wherein:

the first and third low pass filters have substantially the same corner frequency; and

the second and fourth low pass filters have substantially the same corner frequency.

8. (Currently Amended) An apparatus comprising:

first and second differential input nodes;

first and second low pass filters coupled to receive a first signal from the first differential input node;

third and fourth low pass filters coupled to receive a second signal from the second differential input node; and

a differential amplifier including first and second input transistors to form a first differential input stage, and third and fourth input transistors to form a second differential input stage, the first and second differential input stages coupled in parallel, wherein the first and third low pass filters are coupled to provide signals to the first and second input transistors, respectively, of the first differential input stage, and the second and fourth low pass filters are coupled to provide signals to the third and fourth input transistors, respectively, of the second differential input stage. ~~with two parallel input stages coupled to the first, second, third, and fourth low pass filters.~~

9. (Original) The apparatus of claim 8 wherein at least one of the first, second, third, and fourth low pass filters has a programmable response.

10. (Original) The apparatus of claim 8 further comprising an automatic gain control circuit having a transistor to shunt a pair of differential output nodes from the differential amplifier.

11. (Original) The apparatus of claim 10 wherein the automatic gain control is coupled to sense a voltage on the first and second differential input nodes.

12. (Original) The apparatus of claim 10 wherein the automatic gain control is coupled to sense a voltage on the differential output nodes of the differential amplifier.

13. (Original) The apparatus of claim 8 further comprising an input amplifier coupled to receive an input signal and to drive the first and second differential input nodes.

14. (Original) The apparatus of claim 13 wherein the first and third low pass filters exhibit a corner frequency corresponding to a first corner frequency of a band pass response, and the second and fourth low pass filters exhibit a corner frequency corresponding to a second corner frequency of the band pass response.

15-28. (Canceled)